AMENDMENTS TO THE CLAIMS PRESENTED ON DECEMBER 08, 2008 IN RESPONSE TO THE NON-FINAL OFFICE ACTION MAILED ON JULY 09, 2008

1. (Currently Amended) An integrated circuit comprising:

a semiconductor substrate;

a buried insulation layer directly over the semiconductor substrate;

a first semiconductor mesa over the buried insulation layer;

a first guard ring substantially surrounding the first semiconductor mesa, wherein the first guard ring extends through the buried insulation layer contacting the semiconductor substrate, and wherein the first guard ring is arranged to provide RF isolation for the first semiconductor mesa;

a second guard ring substantially surrounding the second semiconductor mesa, wherein the second guard ring extends through the buried insulation layer contacting the semiconductor substrate, and wherein the second guard ring is arranged to provide RF isolation for the second semiconductor mesa; and,

a third guard ring between the first and second guard rings, wherein the third guard ring is in contact with the semiconductor substrate, and wherein the third guard ring is arranged to provide further RF isolation for the first and second semiconductor mesas.

2. (Original) The integrated circuit of claim 1 wherein the semiconductor substrate comprises a high resistivity semiconductor substrate.

3. (Currently Amended) The integrated circuit of claim 1 wherein the semiconductor substrate comprises a silicon substrate, wherein the buried insulating layer comprises a buried silicon oxide layer, and wherein the first semiconductor mesa comprises a silicon mesa, and wherein the second semiconductor mesa comprises a silicon mesa.

4. (Original) The integrated circuit of claim 3 wherein the silicon substrate comprises a high resisitivity silicon substrate.

5. (Currently Amended) The integrated circuit of claim 1 wherein the semiconductor substrate is doped in an area that is contacted by the first guard ring, and wherein the semiconductor substrate is doped in an area that is contacted by the second guard ring.

6. (Original) The integrated circuit of claim 5 wherein the semiconductor substrate comprises a high resitivity semiconductor substrate.

7. (Currently Amended) The integrated circuit of claim 5 wherein the semiconductor substrate comprises a silicon substrate, wherein the buried insulating layer comprises a buried silicon oxide layer, ~~and~~ wherein the first semiconductor mesa comprises a silicon mesa, and wherein the second semiconductor mesa comprises a silicon mesa.

8. (Original) The integrated circuit of claim 7 wherein the silicon substrate comprises a high resisitivity silicon substrate.

9. (Currently Amended) The integrated circuit of claim 1 further comprising: ~~an~~

a first insulating ring between the first guard ring and the first semiconductor mesa, wherein the first insulating ring surrounds the first semiconductor mesa; and

a second insulating ring between the second guard ring and the second semiconductor mesa, wherein the second insulating ring surrounds the second semiconductor mesa.

10. (Original) The integrated circuit of claim 9 wherein the semiconductor substrate comprises a high resistivity semiconductor substrate.

11. (Currently Amended) The integrated circuit of claim 9 wherein the semiconductor substrate comprises a silicon substrate, wherein the buried insulating layer comprises a buried silicon oxide layer, wherein the first insulating ring comprises a silicon oxide insulating ring, wherein the second insulating ring comprises a silicon oxide insulating ring, wherein the first semiconductor mesa comprises a silicon mesa, and wherein the second semiconductor mesa comprises a silicon mesa.

12. (Original) The integrated circuit of claim 11 wherein the silicon substrate comprises a high resistivity silicon substrate.

13. (Currently Amended) The integrated circuit of claim 9 wherein the semiconductor substrate is doped in an area that is contacted by the first guard ring, and wherein the semiconductor substrate is doped in an area that is contacted by the second guard ring.

14. (Original) The integrated circuit of claim 13 wherein the semiconductor substrate comprises a high resistivity semiconductor substrate.

15. (Currently Amended) The integrated circuit of claim 13 wherein the semiconductor substrate comprises a silicon substrate, wherein the buried insulating layer comprises a buried silicon oxide layer, wherein the first insulating ring comprises a silicon oxide insulating ring, wherein the second insulating ring comprises a silicon oxide ring, wherein the first semiconductor mesa comprises a silicon mesa, and wherein the second semiconductor mesa comprises a silicon mesa.

16. (Original) The integrated circuit of claim 15 wherein the silicon substrate comprises a high resistivity silicon substrate.

17. (Currently Amended) The integrated circuit of claim 1 wherein the first guard ring comprises a low resistivity guard ring, and wherein the second guard ring comprises a low resistivity guard ring.

18. (Currently Amended) The integrated circuit of claim 1 wherein the first guard ring comprises a metal guard ring, and wherein the second guard ring comprises a metal guard ring.

19. (Currently Amended) The integrated circuit of claim 18 wherein the first and second metal guard rings comprise[[~~s~~]] [[~~a~~]] tungsten guard rings.

20-39. (Withdrawn)

40. (New) The integrated circuit of claim 1, wherein the third guard ring is a low resistivity guard ring.

41. (New) The integrated circuit of claim 1, wherein the first semiconductor mesa is one of a first group of semiconductor mesas, wherein the first guard ring individually surrounds each semiconductor mesa in the group of semiconductor mesas, and wherein the third guard ring surrounds the first guard ring.